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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

William P. MOORE, et al.

Serial No.: 09/805,200 Group Art Unit: 2183

Filed: March 14, 2001 Examiner: Eric Coleman

For: MICROPROCESSOR INCLUDING MICROCODE UNIT THAT ONLY CHANGES THE VALUE OF CONTROL SIGNALS REQUIRED FOR THE CURRENT CYCLE OPERATION FOR REDUCED POWER CONSUMPTION AND METHOD THEREOF

Honorable Commissioner of Patents
Alexandria, VA 22313-1450

SUPPLEMENTAL APPELLANTS' BRIEF ON APPEAL

Sir:

Appellants respectfully appeal the rejection of claims 1-4, 6, 9, 20, and 23-30 in the Office Action mailed July 19, 2005, which reopened prosecution after the filing of an Appeal Brief (but before the Examiner's Answer or decision by the Board).

To summarize, a Notice of Appeal was filed timely on Monday, February 14, 2005 (since the due date of February 13, 2005 fell on a weekend). An Appeal Brief was timely filed on April 14, 2005.

A non-final Office Action mailed July 19, 2005 was issued in response to the Appeal Brief. The non-final Office Action reopened prosecution because of a new ground of rejection of dependent claims 6 and 30. However, the rejection of claims 1-4, 9, 20, and 23-29 remained the same as the rejections applied in the final Office Action mailed October 13,

2004, from which the previous Appeal was taken. No Examiner's Answer was issued by the Office.

As mentioned above, Appellants respectfully appeal the rejection of claims 1-4, 6, 9, 20, and 23-30 in the Office Action mailed July 19, 2005, which reopened prosecution after the filing of an Appeal Brief (but before the Examiner's Answer or decision by the Board).

A Petition to Reinstate Appeal under 37 C.F.R. § 1.181 is being filed concurrently herewith.

Appellants' Brief on Appeal, which was filed timely on April 14, 2005, is incorporated herewith in its entirety.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, assignee of 100% interest of the above-referenced patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-4, 6, 9, 20, and 23-30, all of the claims in the Application, are set forth fully in the attached Appendix.

Claims 1-4, 6, 9, 20, and 23-30 stand rejected on prior art grounds.

Particularly, Claim 20 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Damouny (U.S. Patent No. 4,713,750). Claims 1-4, 9, and 23-29 stand rejected under 35 U.S.C. § 103(s) as being unpatentable over Damouny in view of Thoma (U.S. Patent No. 4,484,268). Claims 6 and 30 stand rejected under 35 U.S.C. § 103(s) as being unpatentable over Damouny in view of Thoma, and further in view of Catherwood, et al. (U.S. Patent No. 5,457,802).

Appellants respectfully appeal the rejections of Claim 20 under 35 U.S.C. § 102(b) as being anticipated by Damouny, Claims 1-4, 9, and 23-29 under 35 U.S.C. § 103(s) as being unpatentable over Damouny in view of Thoma, and Claims 6 and 30 under 35 U.S.C. § 103(s) as being unpatentable over Damouny in view of Thoma, and further in view of Catherwood, which are the sole issues in this Appeal.

IV. STATUS OF AMENDMENTS

An Amendment under 37 C.F.R. § 1.116 was filed on December 13, 2004. Claim 23 was amended merely to add proper punctuation (i.e., a "colon") after the term "*comprising*" in line 2 of claim 23.

An Advisory Action mailed January 4, 2005 entered the Amendment under 37 C.F.R. § 1.116 filed on December 13, 2004, but held claims 1-4, 6, 9, 20, and 23-30 unpatentable. A Notice of Appeal was filed timely on Monday, February 14, 2005, since the due date of February 13, 2005 fell on a weekend. An Appeal Brief was timely filed on April 14, 2005.

Therefore, the claims are pending as set forth in the Appendix.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The invention, as set forth and defined by independent claim 1 is directed to a microprocessor, a microcode unit in a microprocessor, and a method of providing a state machine decoding.

Referring to the exemplary embodiments of the invention depicted in Figures 3A-5, a microprocessor according to an illustrative aspect of the present invention, as exemplarily defined by independent claim 1, includes a microprocessor, including a microcode unit (e.g., 32; see specification at page 7, lines 27-29; and page 8, lines 1-4) for outputting control signals, for each of a plurality of instructions, required by the microprocessor for executing the instructions. Referring to Figure 3B, the microcode unit (e.g., sub-unit 321 of microcode unit 32) includes an instruction address input (schematically shown in Figures 3B) for receiving an instruction address (e.g., address comparator 3211 for receiving a microcode address signal; see specification at page 8, lines 20-22), a control variable input (schematically shown in Figures 3B) for receiving a control variable (e.g., logic signals; see specification at page 9, lines 6-10) corresponding to a current state of the microprocessor, a control signal input (schematically shown in Figures 3B) for receiving all the control signals output by the microcode unit for an immediately preceding instruction (e.g., previous control signals; see specification at page 9, lines 2-5) and a plurality of embedded logic circuits (e.g., 3215) each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals required for executing the received instruction (e.g., see specification at page 9, lines 6-10).

Referring now to Figure 3C, as exemplarily defined by claim 2, each of the embedded logic circuits (e.g., 3215) can include a table (e.g., 32151, as shown in Figures 3C) for performing a table lookup in response to a received instruction, and a controller (schematically shown in Figures 3C) responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup for controllably setting each of the control signals required by the microprocessor for executing the received instruction (e.g., see specification at page 12, lines 8-17).

Referring again to Figure 3B, as exemplarily defined by claim 3, the controller can include means for setting a control signal to a "1" (e.g., 3212) regardless of its immediately preceding value, means for setting a control signal to a "0" (e.g., 3213) regardless of its immediately preceding value, and means for not modifying a control signal from its immediately preceding value (e.g., 3214)(see also, specification at page 12, lines 18-23; see also page 8, lines 20-30 and page 9, line 1).

Referring again to Figure 3B, as exemplarily defined by claim 4, the controller can further include means for setting a control signal to a data state (e.g., see specification at page 12, lines 22-23).

Referring again to Figure 3B, as exemplarily defined by claim 6, the controller also can include means for determining which of the control signals are not to be modified for each instruction (e.g., see specification at page 12, lines 11-27).

Referring again to Figure 3C, as exemplarily defined by claim 9, a microcode unit (e.g., 32; see specification at page 7, lines 27-29; and page 8, lines 1-4) in a microprocessor, for outputting control signals (e.g., see Figure 3A), for each of a plurality of instructions,

required by the microprocessor for executing the instructions. The microcode unit (e.g., sub-unit 321 of microcode unit 32) can include an instruction address input (e.g., address comparator 3211 for receiving a microcode address signal; see specification at page 8, lines 20-22) for receiving an instruction address, a control variable input (schematically shown in Figures 3B) for receiving a control variable (e.g., logic signals; see specification at page 9, lines 6-10) corresponding to a current state of the microprocessor, a control signal input (schematically shown in Figures 3B) for receiving all the control signals output by the microcode unit for an immediately preceding instruction (e.g., previous control signals; see specification at page 9, lines 2-5), and a plurality of embedded logic circuits (e.g., 3215) each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals required for executing the received instruction (e.g., see specification at page 9, lines 6-10).

Referring to Figures 3D-4B, as exemplarily defined by independent claim 20, a method of providing a state machine decoding, includes decoding a current opcode (e.g., step 301) to provide a decode (e.g., see specification at page 13, line 30, and page 14, lines 1-8), setting required functions signals (e.g., step 302; see specification at page 14, lines 8-9), setting exclusive functions outside of the current opcode to a previous state (e.g., step 303; see specification at page 14, lines 10-11), and latching results of the decode (e.g., step 304; see specification at page 14, line 11).

Turning again to the microprocessor according to the claimed invention, as exemplarily defined by claim 23, and referring again to Figure 3C, each of the plurality of embedded logic circuits includes a controller (schematically shown in Figures 3C) for

controllably setting each of the control signals required by the microprocessor for executing the received instruction (e.g., see specification at page 12, lines 11-23).

Referring again to Figure 3C, as exemplarily defined by claim 24, each of the plurality of embedded logic circuits includes a controller (schematically shown in Figures 3C) for controllably setting only each of the control signals required by the microprocessor for executing the received instruction (e.g., see specification at page 12, lines 11-23).

Referring again to Figure 3C, as exemplarily defined by claim 25, each of the plurality of embedded logic circuits includes a table (e.g., 32151, as shown in Figures 3C) that performs a table lookup in response to a received instruction (e.g., see specification at page 12, lines 8-17).

Referring again to Figure 3C, as exemplarily defined by claim 26, the controller is responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup (e.g., see specification at page 12, lines 18-23; see also page 8, lines 20-30 and page 9, line 1).

Referring again to Figures 3B and 3C, as exemplarily defined by claim 27, the controller includes means for maintaining a control signal at an immediately preceding value of the control signal (see also, specification at page 12, lines 18-23; see also page 8, lines 20-30 and page 9, line 1).

Referring again to Figures 3B and 3C, as exemplarily defined by claim 28, the controller further includes means (e.g., 3212) for setting a control signal to a "1" regardless of an immediately preceding value of the control signal, and means (e.g., 3213) for setting a

control signal to a "0" regardless of an immediately preceding value of the control signal (see also, specification at page 12, lines 18-23; see also page 8, lines 20-30 and page 9, line 1).

Referring to Figures 3B and 3C, as exemplarily defined by claim 29, the controller further includes means (e.g., 3214) for setting a control signal to a data state (e.g., see specification at page 12, lines 22-23).

Referring to Figures 3B and 3C, as exemplarily defined by claim 30, the controller can further include means (e.g., 3214) for determining at least one of the control signals to be maintained for each instruction (see also, specification at page 12, lines 18-23; see also page 8, lines 20-30 and page 9, line 1).

In the claimed invention, in addition to the "0" or "1" value which can be set for each control signal, the previous value can also be set, thereby reducing the power within the microprocessor (e.g., see specification at page 10, lines 2-5).

Specifically, since each function is a function of a microcode address, by only changing the value of control signals that are absolutely required for that particular microcode address (e.g., ADD, STORE, MULT etc. as determined by the decoding), the power of the microprocessor can be minimized since node toggle, as discussed above, is greatly reduced as compared to the conventional machines and systems (e.g., see specification at page 10, lines 6-11).

For example, in an exemplary embodiment of the claimed invention, the power savings was on the order of about 30-40% over the conventional systems. Hence, if the function remains the same from a previous opcode to the next opcode (and hence from cycle-to-cycle), then the previous value may be maintained again, and no node toggle results since

values are not being changed from high to low or from low to high (e.g., see specification at page 10, lines 11-16).

Thus, with the claimed invention, each opcode becomes a function of the previous opcode and only conflicting (e.g., required) control signals must be resolved, thereby greatly reducing power consumption (e.g., see specification at page 10, lines 17-19).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for review by the Board of Patent Appeals and Interferences are whether Claim 20 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Damouny and whether Claims 1-4, 9, and 23-29 stand rejected under 35 U.S.C. § 103(s) as being unpatentable over Damouny in view of Thoma, and Claims 6 and 30 stand rejected under 35 U.S.C. § 103(s) as being unpatentable over Damouny in view of Thoma, and further in view of Catherwood.

VII. ARGUMENT

In the Response to Arguments of the Office Action mailed July 19, 2005, which reopened prosecution, the Examiner addressed the arguments set forth in the Appeal Brief.

To summarize, Appellants submit that the Examiner's position is flawed as a matter of fact and law. Thus, Claim 20 is not anticipated by, or rendered obvious from, Damouny, Claims 1-4, 9, and 23-29 also are not rendered obvious from Damouny in view of Thoma, and Claims 6 and 30 are not rendered obvious from Damouny in view of Thoma, and further in view of Catherwood.

A **Claim 20 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Damouny.**

THE EXAMINER'S POSITION

In the Response to Arguments of the Office Action mailed July 19, 2005, which reopened prosecution, the Examiner addressed the arguments set forth in the Appeal Brief.

Particularly, with respect to claim 20, the Examiner stated that "*claim 20 provides for setting required function signals. For (sic) an instruction to be operational it must set the "required function signals". So therefore inherently the signals shown in the Damouny reference that are set and described in the outstanding rejection comprise the required functions signals. Claim 20 provides for setting exclusive functions outside the current opcode to a previous state. Here Damouny taught that the function signals for the previous instruction are set or latched during the Processing of the current instruction as discussed in the outstanding rejection. Here for e a previous instruction that is identical to the current instruction would inherently contain functions that differed at least partially from the functions of the Current instruction. Since Damouny taught setting or latching the previous instruction function signals of the previous instruction during a current instruction then this (sic) requires that the exclusive functions outside of the current opcode would have been set. The latching is taught by Damouny as discussed in the outstanding rejection. Claim 20 does not include any limitation that requires that only changing the value of signals that are absolutely required for a particular microcode address. Note there is not limitation as to which instruction (e.g., current or previous) (with exclusive functions outside the current*

opcode) are the exclusive functions included." (see Office Action at pages 14-15, bridging paragraph).

APPELLANTS' POSITION

For the following reasons, Appellants respectfully submit that the Examiner's position is flawed as a matter of fact and law, and therefore, traverse this rejection.

For example, claim 20 recites, *inter alia*, a method of providing a state machine decoding, comprising:

> *decoding a current opcode to provide a decode;*
> *setting required functions signals;*
> *setting exclusive functions outside of the current opcode to a previous state; and*
> *latching results of the decode* (emphasis added).

That is, according to the claimed invention, each opcode becomes a function of the previous opcode (e.g., see specification at page 10, lines 17-19). In other words, by setting required functions signals of the current opcode, and also setting exclusive functions which are outside of the current opcode to a previous state, the current opcode becomes a function of the previous opcode. Thus, only conflicting control signals (e.g., required control signals) must be resolved and the power consumption can be greatly reduced (e.g., see specification at page 10, lines 18-19).

In comparison, Damouny clearly does not disclose or suggest the claimed combination of "*setting required functions signals*" and also "*setting exclusive functions outside of the current opcode to a previous state*" as recited in claim 20.

Instead, Damouny simply teaches that every control signal is modified for each instruction. That is, Damouny does not disclose, suggest, or even contemplate *which* of the

function signals would be set. Indeed, Damouny does not disclose, suggest, or even address the problems being solved by the claimed invention.

Thus, Appellants respectfully submit that by simply teaching that every control signal is modified for each instruction, and not even contemplating *which* of the function signals would be set, Damouny clearly does not disclose or suggest the claimed combination of "*setting required functions signals*" and also "*setting exclusive functions outside of the current opcode to a previous state*" as recited in claim 20.

In comparison, the claimed invention discloses that, since each function is a function of a microcode address, by only changing the value of control signals that are absolutely *required* for that particular microcode address (e.g., ADD, STORE, MULT etc. as determined by the decoding), the power of the microprocessor can be minimized and node toggle can be greatly reduced as compared to the conventional machines and systems (e.g., see specification at page 10, lines 6-11).

For at least the foregoing reasons, Appellants respectfully submit that Damouny neither discloses nor suggests all of the features of independent claim 20, and therefore, respectfully request that the Examiner withdraw this rejection and permit claim 20 to pass to immediate allowance.

B. Claims 1-4, 9, and 23-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Damouny in view of Thoma.

For the following reasons, Appellants respectfully submit that the Examiner's position is flawed as a matter of fact and law, and therefore, traverse this rejection.

i) Independent Claim 1

THE EXAMINER'S POSITION

With respect to claim 1, the Examiner stated that "*the claim only requires that for one (i.e., preceding) instruction all the control signals have to be input to the microcode unit. The Damouny reference clearly disclosed that all the control signals required for a branch instruction was input to the microcode unit as discussed in the outstanding rejection. Here, as the branch control signals provide for addressing an (sic) immediately succeeding instruction, the control signals for the branch (or immediately preceding instruction) is input to the microcode unit*" (see Office Action at pages 15-16, bridging paragraph).

APPELLANTS' POSITION

For the reasons set forth below, Appellants respectfully reiterate that Damouny and Thoma, either individually or in combination, do not disclose, suggest, or even mention these features of the claimed invention, or for that matter, the advantages derived from the unique combination of structural features recited in the claimed invention.

For example, as mentioned above, the claimed invention provides a novel and unique combination of elements in which, since each function is a function of a microcode address, by only changing the value of control signals that are absolutely required for that particular microcode address (i.e., as exemplarily defined by dependent claim 24) (e.g., ADD, STORE, MULT etc. as determined by the decoding), the power of the microprocessor can be minimized since node toggle, as discussed above, is greatly reduced as compared to the conventional machines and systems (e.g., see specification at page 10, lines 6-11). That is, in an exemplary aspect of the claimed invention, each opcode becomes a function of the

previous opcode and only conflicting (e.g., required) control signals must be resolved, thereby greatly reducing power consumption (e.g., see specification at page 10, lines 17-19).

With respect to independent claim 1, Appellants reiterate that independent claim 1 would not have been obvious from Damouny in view of Thoma.

For example, independent claim 1 recites, *inter alia*, a microprocessor, comprising:

> a microcode unit for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit comprising:
>
> *an instruction address input for receiving an instruction address;*
> *a control variable input for receiving a control variable corresponding to a current state of the microprocessor;*
> *a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction; and*
> *a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals required for executing said received instruction*
> (emphasis added).

Appellants submits that it would not have been obvious to modify Damouny in view of Thoma since, by teaching that every control signal is modified for each instruction, Damouny would teach away from the claimed invention. Moreover, if Damouny were modified to arrive at the claimed invention, such a modification clearly would require a change in the principle of operation of the device of Damouny.

As mentioned above, independent claim 1 recites, *inter alia*, a microcode unit including "*a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction*" (emphasis added).

However, with respect to the signal 182 of Damouny, Appellants respectfully submit that Damouny merely discloses that "*[t]he input signals that control the internal state of the branch PLA arrive on the bus 182 as the branch select field and on the bus 184 representing various internal and external branch conditions such as overflow, interrupt, abort, etc.*" (see Damouny at column 4, lines 57-61; see also Figure 1A), not that a control signal input receives "***all*** *the control signals output by the microcode unit for an immediately preceding instruction*" as claimed in claim 1.

Thus, Appellants respectfully submit that Damouny and Thoma, either individually or in combination, do not disclose or suggest all of the features of independent claim 1 of the present application.

ii) Dependent Claims 2-4

THE EXAMINER'S POSITION

With respect to claims 2-4, the Examiner noted that "*for the limitation of means for not modifying a control signal from its (sic) immediately preceding value. This claim limitation only requires that the value is not modified so if the system sets the same value for a signal of succeeding instruction to the same value a preceding instruction, the Examiner contends that the value has not been modified and therefore meets the claim limitation*" (see Office Action at page 16, first full paragraph).

APPELLANTS' POSITION

First, Appellants reiterate that dependent claims 2-4 also should be patentable at least by virtue of their dependency from claim 1, as well as for the additional recitations recited therein.

For example, dependent claim 3 recites, *inter alia*, that the controller includes:

> *means for setting a control signal to a "1" regardless of its immediately preceding value;*
> *means for setting a control signal to a "0" regardless of its immediately preceding value; and*
> *means for not modifying a control signal from its immediately preceding value* (emphasis added).

The specification clearly describes that, in addition to the "0" or "1" value which can be set for each control signal, the previous value can also be set, thereby reducing the power within the microprocessor (e.g., see specification at page 10, lines 2-5).

As mentioned above, the Examiner alleges that "*when the control signal of mention does not change from one instance to the next, the control signal is set to the same value as before and is not modified from the previous value, but is modified to retain the value*".

However, Damouny and Thoma, individually or in combination, do not disclose or suggest maintaining and/or retaining the previous value. Instead, these references simply teach that every control signal is modified for each instruction.

Such clearly does not imply that Damouny or Thoma disclose or suggest "*means for not modifying a control signal from its immediately preceding value*" as claimed and disclosed in the present application. Indeed, the Examiner has not cited any structure, equivalents thereof, or identity of function necessary for the claimed "*means for not modifying a control signal from its immediately preceding value*", as disclosed in the present application.

In comparison, the disclosure of the present application exemplarily describes that the output signal of the address comparator 3211 is issued to AND gate 3212 (e.g., for the "1"

block), AND gate 3213 (e.g., for the "0" block), and to AND gate 3214 (e.g., see specification at page 8, lines 24-30 and page 9, line 1).

Thus, Appellants respectfully submit that claim 3 clearly would not have been obvious over Damouny and Thoma, either individually or in combination.

iii) Dependent Claims 23-29

THE EXAMINER'S POSITION

With respect to dependent claims 23-30, the Examiner "*contends that Damouny and Thoma clearly shows as the opcode is decoded by a plurality of PLAs in parallel and only the signals form the selected PLA are output from the PLA for latching, setting and use by the system (see fig. 1 of Thoma and the outstanding rejection above). Since the Thoma teaching of selecting the functions by class provide then a smaller number of lines to specify a particular function then the intended use of limiting the number of function signals that are set is indeed realizable. The Examiner contends the number of functions per class is specific the particular implementation and the limit of only one function to some (sic) classes is not precluded by the Thoma teachings*" (see Office Action at pages 16-17, bridging paragraph).

APPELLANTS' POSITION

With respect to claims 23-29, the Examiner rejects these claims as being unpatentable over Damouny in view of Thoma. However, Appellants respectfully submit that claims 23-29 would not have been obvious from Damouny and Thoma, individually or in combination. Therefore, Appellants traverse the rejection of these claims.

For example, dependent claim 24 recites, *inter alia*, that "*each of the plurality of embedded logic circuits comprises a controller for controllably setting only each of the*

control signals required by the microprocessor for executing said received instruction"

(emphasis added).

The Examiner alleges that Figure 1A of Damouny discloses this feature of the claimed invention. However, as the Examiner also acknowledged in the Office Action mailed on April 16, 2004, in the final Office Action mailed October 13, 2004, and in the Advisory Action mailed January 4, 2005, Damouny discloses that "*every control signal is modified for each instruction*".

Thus, Damouny clearly does not disclose or suggest "*a controller for controllably setting only each of the control signals required by the microprocessor for executing said received instruction*" as recited in claim 24. Indeed, the Examiner acknowledged this distinction between the modifying every control signal for each instruction and "*controllably setting only each of the control signals required by the microprocessor for executing said received instruction*", as recited in claim 24 (see Advisory Action at Continuation Sheet).

On the other hand, the Examiner asserted in the present Office Action that Thoma teaches this feature. As mentioned above, the Examiner alleged that "*the number of functions per class is specific the particular implementation and the limit of only one function to some (sic) classes is not precluded by the Thoma teachings*" (see Office Action at pages 16-17, bridging paragraph; emphasis Appellants).

However, Appellants submit that it is not enough that Thoma allegedly does not "preclude" including the features of the claimed invention. Instead, Appellants respectfully submit that Thoma must actually teach the missing features (i.e., make up for the deficiencies

of Damouny). Moreover, modifying Damouny based on such teachings of Thoma also must have been obvious from Damouny and Thoma or the art in general.

Appellants submit that Damouny and Thoma, either individually or in combination, clearly do not disclose or suggest "*a controller for controllably setting only each of the control signals required by the microprocessor for executing said received instruction*" as recited in claim 24.

With respect to claim 27, the Examiner "*contends that the claim only requires that for one (i.e., preceding) instruction all the control signals have to be input to the microcode unit. The Damouny reference clearly disclosed that all the control signals required for a branch instruction was input to the microcode unit (as discussed in the outstanding rejection). Here, as the branch control signals provide for the addressing an (sic) immediately succeeding instruction, the control signals for the branch (or immediately preceding instruction) is input to the microcode unit (see fig. 1A of Damouny). Also as detailed in the outstanding rejection as the succeeding instruction is being processed the preceding instruction control signals are being set of latched (sic)*" (see Office Action at page 17, paragraph (f)).

In comparison, dependent claim 27 recites, *inter alia*, that "*the controller includes means for maintaining a control signal at an immediately preceding value of said control signal*" (emphasis added).

However, as mentioned above, Damouny and Thoma, individually or in combination, do not disclose or suggest maintaining and/or retaining the previous value. Particularly, neither Damouny or Thoma discloses or suggests the claimed "*means for maintaining*" as disclosed in the present application.

Instead, the references simply teach that *every* control signal is modified for each instruction. Such clearly does not imply that Damouny or Thoma disclose or suggest "*means for maintaining a control signal at an immediately preceding value of said control signal*" as claimed and disclosed by the present application.

Indeed, the Examiner has not cited any structure, equivalents thereof, or identity of function necessary for the claimed "*means for maintaining a control signal at an immediately preceding value of said control signal*", as disclosed in the present application.

Thus, Appellants respectfully submit that claim 27 is patentable over Damouny and Thoma, either individually or in combination.

For the foregoing reasons, Appellants respectfully submit that Damouny and Thoma, either individually or in combination, do not disclose or suggest all of the features of the claimed invention.

Therefore, the Examiner respectfully is requested to reconsider and withdraw the rejection of these claims and permit claims 1-4, 9, 20, and 23-29 to pass to immediate allowance.

C Claims 6 and 30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Damouny in view of Thoma, and further in view of Catherwood.

THE EXAMINER'S POSITION

With respect to dependent claims 6 and 30, the Examiner acknowledged that Damouny does not expressly disclose or suggest determining which control signals that are

not to be modified for each instruction, as recited in claim 6, and means for determining at least one of the signals to be maintained for each instruction, as recited in claim 30 (see Office Action at page 13, numbered paragraph 23).

However, the Examiner alleged that Catherwood makes up for the deficiencies of Damouny and Thoma (e.g., see Catherwood, at column 3, lines 9-57).

APPELLANTS' POSITION

Appellants respectfully submit, however, that Catherwood does not make up for the deficiencies of Damouny and Thoma. Thus, Appellants traverse this rejection.

Dependent claim 6 recites, *inter alia*, "*means for determining which of the control signals are not to be modified for each instruction*" (emphasis added).

On the other hand, dependent claim 30 recites, *inter alia*, "*means for determining at least one of said control signals to be maintained for each instruction*" (emphasis added).

As mentioned above, Damouny discloses automatically modifying every control signal for each instruction. Since all control signals in Damouny are automatically modified, there is no need (i.e., it is not necessary) to even make such a determination.

Appellants submit, however, that modifying Damouny to include the features of freezing the external buses in their previous state, in some cases, would change the principle of operation of Damouny. That is, if Damouny were modified to include such features of Catherwood, such modifications would change the principle of operation of the Damouny reference.

Thus, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the

references are not sufficient to render the claims pram facie obvious (see In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959); see also M.P.E.P. § 2143.02).

Moreover, even assuming *arguendo* that it would have been obvious to modify the primary references Damouny and Thoma in view of the tertiary reference Catherwood, Appellants submit that the resulting combination still would not disclose or suggest all of the features of the claimed "*means for determining which of the control signals are not to be modified for each instruction*", as recited in claim 6 and disclosed in the present application, and "*means for determining at least one of said control signals to be maintained for each instruction*", as recited in claim 30 and disclosed in the present application.

That is, Catherwood merely discloses that there are times when it is desirable to "freeze" the external control buses in their previous state, and other times when it is desirable to not "freeze" the external control buses in their previous state. Specifically, Catherwood discloses that for bus cycles of an instruction which do not require use of an external address bus, the values driven by the address pins are "frozen" in their previous logic state (e.g., see Catherwood at Abstract).

Catherwood does not, however, disclose or suggest determining which of these external control buses to "freeze", but instead, merely "freezes" all of the external control buses or none at all.

Appellants submit that such is not the same as, or comparable to, the disclosed "*means for determining*", as recited in claims 6 and 30, and as disclosed in the present application. Indeed, the Examiner has not cited any structure, equivalents thereof, or identity of function necessary for the claimed "*means for determining*".

In comparison, referring again to Figure 3B, the present invention discloses that the controller includes means for determining which of the control signals are not to be modified for each instruction (e.g., see specification at page 12, lines 11-27).

Referring to Figures 3B and 3C, the controller can further include means (e.g., 3214) for determining at least one of the control signals to be maintained for each instruction (see also, specification at page 12, lines 18-23; see also page 8, lines 20-30 and page 9, line 1).

In the claimed invention, in addition to the "0" or "1" value which can be set for each control signal, the previous value can also be set, thereby reducing the power within the microprocessor (e.g., see specification at page 10, lines 2-5).

Specifically, since each function is a function of a microcode address, by only changing the value of control signals that are absolutely required for that particular microcode address (e.g., ADD, STORE, MULT etc. as determined by the decoding), the power of the microprocessor can be minimized since node toggle, as discussed above, is greatly reduced as compared to the conventional machines and systems (e.g., see specification at page 10, lines 6-11).

For example, in an exemplary embodiment of the claimed invention, the power savings was on the order of about 30-40% over the conventional systems. Hence, if the function remains the same from a previous opcode to the next opcode (and hence from cycle-to-cycle), then the previous value may be maintained again, and no node toggle results since values are not being changed from high to low or from low to high (e.g., see specification at page 10, lines 11-16).

Thus, with the claimed invention, each opcode becomes a function of the previous opcode and only conflicting (e.g., required) control signals must be resolved, thereby greatly reducing power consumption (e.g., see specification at page 10, lines 17-19).

For the foregoing reasons, Appellants respectfully submit that it would not have been obvious to modify Damouny and Thoma in view of Catherwood, since such a modification would change the principle of operation of the primary reference Damouny. Moreover, even assuming *arguendo* that it would have been obvious to modify the primary references Damouny and Thoma in view of the tertiary reference Catherwood, Appellants submit that the resulting combination still would not disclose or suggest all of the features of the claimed "*means for determining which of the control signals are not to be modified for each instruction*", as recited in claim 6 and disclosed in the present application, and "*means for determining at least one of said control signals to be maintained for each instruction*", as recited in claim 30 and disclosed in the present application.

Thus, Appellants respectfully submit that Damouny, Thoma, and Catherwood, either individually or in combination, do not disclose or suggest all of the features of claims 6 and 30. The Examiner respectfully is requested to reconsider and withdraw the rejection of these claims and permit claims 6 and 30 to pass to immediate allowance.

VIII. CONCLUSION

In view of the foregoing, Appellants submit that claims 1-4, 6, 9, 20, and 23-30, all the claims presently pending in the application, are patentably distinct from the prior art of

record and in condition for allowance. Thus, the Board is respectfully requested to remove the rejections of claims 1-4, 6, 9, 20, and 23-30.

Please charge any deficiencies and/or credit any overpayments necessary to enter this paper to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

Date: October 19, 2005

John J. Dresch, Esq.
Registration No. 46,672

Seam M. McGinn, Esq.
Registration No. 34,386

MCGINN INTELLECTUAL PROPERTY LAW GROUP, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, Virginia 22182-3817
(703) 761-4100
Customer No. 21254

CERTIFICATE OF TRANSMISSION

I certify that I transmitted via facsimile to (571) 273-8300 the enclosed Supplemental Appeal Brief to Examiner Eric Coleman on October 19, 2005.

John J. Dresch, Esq.
Registration No. 46,672

CLAIMS APPENDIX

1. (Previously presented) A microprocessor, comprising:

a microcode unit for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit comprising:

an instruction address input for receiving an instruction address;

a control variable input for receiving a control variable corresponding to a current state of the microprocessor;

a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction; and

a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals required for executing said received instruction.

2. (Original) The microprocessor according to claim 1, wherein each of the embedded logic circuits includes:

a table for performing a table lookup in response to a received instruction; and

a controller responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup for controllably setting each of the control signals required by the microprocessor for executing said received instruction.

3. (Original) The microprocessor of claim 2, wherein the controller includes:

means for setting a control signal to a "1" regardless of its immediately preceding value;

means for setting a control signal to a "0" regardless of its immediately preceding value; and

means for not modifying a control signal from its immediately preceding value.

4. (Original) The microprocessor of claim 3, wherein the controller further includes:

means for setting a control signal to a data state.

5. (Canceled).

6. (Previously presented) The microprocessor according to claim 1, further comprising means for determining which of the control signals are not to be modified for each instruction.

7-8. (Canceled).

9. (Previously presented) A microcode unit in a microprocessor, for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit comprising:

an instruction address input for receiving an instruction address;

a control variable input for receiving a control variable corresponding to a current state of the microprocessor;

a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction; and

a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals required for executing said received instruction.

10-19. (Canceled).

20. (Original) A method of providing a state machine decoding, comprising:

decoding a current opcode to provide a decode;

setting required functions signals;

setting exclusive functions outside of the current opcode to a previous state; and

latching results of the decode.

21-22. (Canceled).

23. (Previously presented) The microprocessor of claim 1, wherein each of the plurality of embedded logic circuits comprises:

a controller for controllably setting each of the control signals required by the microprocessor for executing said received instruction.

24. (Previously presented) The microprocessor of claim 1, wherein each of the plurality of embedded logic circuits comprises a controller for controllably setting only each of the control signals required by the microprocessor for executing said received instruction.

25. (Previously presented) The microprocessor of claim 1, wherein each of the plurality of embedded logic circuits comprises a table that performs a table lookup in response to a received instruction.

26. (Previously presented) The microprocessor of claim 25, wherein said controller is responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup.

27. (Previously presented) The microprocessor of claim 23, wherein the controller includes means for maintaining a control signal at an immediately preceding value of said control signal.

28. (Previously presented) The microprocessor of claim 27, wherein the controller further includes:

means for setting a control signal to a "1" regardless of an immediately preceding value of said control signal; and

means for setting a control signal to a "0" regardless of an immediately preceding value of said control signal.

29. (Previously presented) The microprocessor of claim 28, wherein the controller further comprises means for setting a control signal to a data state.

30. (Previously presented) The microprocessor according to claim 1, further comprising means for determining at least one of said control signals to be maintained for each instruction.

EVIDENCE APPENDIX

Not applicable.

RELATED PROCEEDINGS APPENDIX

Not applicable.